ABSTRACT OF THE DISCLOSURE

The integrated circuit comprises, in addition to a first bus and a first DMA controller, a second bus and a second DMA controller that mutually connects the first bus and the second bus. A main memory is connected to the first bus, and a frame memory is connected to the second bus.

By the construction, a possible conflict in data transfer as "urgent processing" and as "normal processing" can be avoided. The data transfer as "urgent processing" includes transferring image data between the frame memory and an image input device or an image display device; while the data transfer as "normal processing" includes transferring image data between the main memory and the frame memory.